CLK_SHR
PHS_CNTL
RESET_VIT
LINKCLK
INTER_CLK
PHS_CNTL
ADRS_RST
TRNS_CLK
VME80
BSCN_CLK
BX0'
QB_PHS
TOPCK160
BOTCK160
TOPCK120
BOTCK120
ERR_PHS0
ERR_PHS1
ERR_PHS_CK0
ERR_PHS_CK1
ERR_PHS_CK2
JETCLK
ADDER_CLK
MUX_SEL
BSCN
BUF_CLK
MEMCLK
EISO_CLOCK

Changes	By	Date	Drawn JLL	Project CMS CAL TRIGGER PROCESSOR
			Date 28/1/97	RECEIVER CARD
			CHK'D	BLOCK: CLK_RST
			Scale	High Energy Physics
REVB	JLL	6/12/02	D0671	University of Wisconsin
REVA	JLL	27/04/01		