EDGE_RD
MID_RD
TDI
TDO
TAP_CNTL
LR_OUT
TB_IN
LR_IN
U197
BSCAN ASIC_MSB
U177
BSCAN ASIC_LSB
USE R1 TO GENERATE THE INT_CNR SIGNALS.
SWAP
SHR_LR
MID
EDGE
CLK
RESET
DLY_CNTL

Changes	By	Date	Drawn JLL	Project CMS CAL TRIGGER PROCESSOR
			Date 12/4/01	RECEIVER CARD
			CHK'D	BLOCK: DRVRS_R0_L
			Scale	High Energy Physics
REVB	JLL	6/12/02	D0724	University of Wisconsin