EDGE_RD
MID_RD
TDI
TDO
TAP_CNTL
RCVR_Ø1
RCVR_ODD
BSCN_TMS
BSCN_TRST
BSCN_TDX0
BSCN_TDX1
MEM3
MEM4
MEM5
MEM6
MEM0
MEM1
MEM2
MEM7
R48
49.9
R269
net299
ADD_REF
VTT
TB_OUT
TB_IN
U198
U178
BSCAN ASIC_MSB
BSCAN ASIC_LSB
U34
U33
MC100E158FN
MUX
Sel
C43
.01uF
C322
C287
C300
C309
C50
C297
C264
C263
C265
C273
C53
C54
R271
R281
R300
R257
R232
R240
R231
R267
R268
R270
R233
RN3
R98
R61
R0R_TB_OUT4
R0R_TB_OUT5
R0R_TB_OUT6
R0R_TB_OUT7
R0R_TB_IN4
R0R_TB_IN5
R0R_TB_IN6
R0R_TB_IN7
TB_TO_CB0
TB_TO_CB1
TB_TO_CB2
TB_TO_CB3
LR_TO_CB0
LR_TO_CB1
LR_TO_CB2
LR_TO_CB3
TB_SHR_IN0
TB_SHR_IN1
TB_SHR_IN2
TB_SHR_IN3
LR_SHR_IN0
LR_SHR_IN1
LR_SHR_IN2
LR_SHR_IN3
MID_IN0
MID_IN1
MID_IN2
MID_IN3
EDGE_IN0
EDGE_IN1
EDGE_IN2
EDGE_IN3
LCL_DLY0
LCL_DLY1
LCL_DLY2
SHR_DLY0
SHR_DLY1
SHR_DLY2
SHR_LR
BOT_CNR0
BOT_CNR1
BOT_CNR2
BOT_CNR3
BOT_OUT0
BOT_OUT1
BOT_OUT2
BOT_OUT3
TOP_CNR0
TOP_CNR1
TOP_CNR2
TOP_CNR3
TOP_OUT0
TOP_OUT1
TOP_OUT2
TOP_OUT3
NBR_LR0
NBR_LR1
NBR_LR2
NBR_LR3
MID_OUT0
MID_OUT1
MID_OUT2
MID_OUT3
EDGE_OUT0
EDGE_OUT1
EDGE_OUT2
EDGE_OUT3
CLK
RESET
MS_NIB
SHP_IN
LOVR_SHP
ROVR_SHP
MID_SHP0
MID_SHP1
MID_SHP2
MID_SHP3
EDGE_SHP0
EDGE_SHP1
EDGE_SHP2
EDGE_SHP3
VREF
ENB_MEM
PCODE0
PCODE1
PCODE2
PCODE3
TMS
TRST
TCK
TDO
TDI
MID_MEM0
MID_MEM1
MID_MEM2
MID_MEM3
EDGE_MEM0
EDGE_MEM1
EDGE_MEM2
EDGE_MEM3
EDG_MUX_RØ
BOT_CNR
BOT_OUT
TOP_CNR
TOP_OUT
EXT_CNR
INT_CNR
SWAP
MID
EDGE
CLK
RESET
DLY_CNTL
CLK_ROR_MSB
CLK_ROR_LSB
LOVR_SWP1
ROVR_SWP1
RØ_MID_SWP0
RØ_MID_SWP1
RØ_MID_SWP2
RØ_MID_SWP3
RØ_MID_SWP4
RØ_MID_SWP5
RØ_MID_SWP6
RØ_MID_SWP7
RØ_EDG_SWP0
RØ_EDG_SWP1
RØ_EDG_SWP2
RØ_EDG_SWP3
RØ_EDG_SWP4
RØ_EDG_SWP5
RØ_EDG_SWP6
RØ_EDG_SWP7
EISCK0
EISCK1
EISCK2
EISCK3
EISCK4
EISCK5
EISCK6
EISCK7
EISDI0
EISDI1
EISDI2
EISDI3
EISDI4
EISDI5
EISDI6
EISDI7
J2 a27
J2 b27
J2 c27
J2 d27
J2 a28
J2 b28
J2 c28
J2 d28
J2 a23
J2 b23
J2 c23
J2 d23
J2 a24
J2 b24
J2 c24
J2 d24
J2 a31
J2 b31
J2 c31
J2 d31
J2 a32
J2 b32
J2 c32
J2 d32
J2 a35
J2 b35
J2 c35
J2 d35
J2 a36
J2 b36
J2 c36
J2 d36
J2 a29
J2 b29
J2 c29
J2 d29
J2 a30
J2 b30
J2 c30
J2 d30
J2 a33
J2 b33
J2 c33
J2 d33
J2 a34
J2 b34
J2 c34
J2 d34

Changes	By	Date	Drawn JLL	Project CMS CAL TRIGGER PROCESSOR
			Date 12/4/01	RECEIVER CARD
			CHK'D	BLOCK: DRVRS_RØ_R
			Scale	High Energy Physics
REVB	JLL	6/12/02	D0725	University of Wisconsin