EDGE_RD
MID_RD
TDI
TDO
TAP_CNTL
RCVR_ODD
TB_OUT
TB_IN
U199
BSCAN ASIC_MSB
U179
BSCAN ASIC_LSB
EDG_MUX_R1
BOT_CNR
BOT_OUT
TOP_CNR
TOP_OUT
SWAP
MID
EDGE
CLK
RESET
DLY_CNTL

Changes	By	Date	Drawn JLL	Project CMS CAL TRIGGER PROCESSOR
			Date 12/4/01	RECEIVER CARD
			CHK'D	BLOCK: DRVRS_R1_L
			Scale	High Energy Physics
REVB	JLL	6/12/02	D0726	University of Wisconsin