EDGE_RD
MID_RD
TDI
TDO
TAP_CNTL
U2
U1
BSCAN ASIC_MSB
BSCAN ASIC_LSB
TB_IN
INT_CNR
SWAP
MID
EDGE
CLK
RESET
DLY_CNTL

| Changes | By | Date | Drawn JLL | Project CMS CAL TRIGGER PROCESSOR |
|---|---|---|---|---|
| | | | Date 12/4/01 | RECEIVER CARD |
| | | | CHK'D | BLOCK: DRVRS_R1_R |
| | | | Scale | High Energy Physics |
| REVB | JLL | 6/12/02 | D0727 | University of Wisconsin |