MEM_RD
BSCN_BSCN
DLY_CNT
CNR_CNTRL
VTT 74Ω-5Ω
R295
BSCN_TDO
BSCN_TCK1
BSCN_TMS
BSCN_TRST
BSCN_TDI
MEM_SEL
MEM_MUX
SHARE
EISO_IN
EISO_CLOCK
EISO_RST
DRVRS_R0_L
DRVRS_R0_R
DRVRS_R1_L
DRVRS_R1_R
EDGE_RD
MID_RD
TAP_CNTL
TDI
LR_OUT
TB_IN
LR_IN
MID
EDGE
CLK
RESET
DLY_CNTL
TDO
SWAP
SHR_LR
TB_OUT
RCVR_ODD
RCVR_Ø1
INT_CNR
R0_ODD
RECV_Ø1
R1_ODD
net473
net474
net475
MC100E111FN
UN4
CLK_R0L_LSB
CLK_R0L_MSB
CLK_R0R_LSB
CLK_R0R_MSB
CLK_R1L_LSB
CLK_R1L_MSB
CLK_R1R_LSB
CLK_R1R_MSB
R50
49.9
C53
.01uF
net480
R382
U256
MC100E104
net476
net477
net478
net479

Changes	By	Date	Drawn JLL	Project CMS CAL TRIGGER PROCESSOR
			Date 5/11/96	RECEIVER CARD
			CHK'D	BLOCK: EISO_DRVRS
			Scale	High Energy Physics
REV B	JLL	6/12/02	D0639	University of Wisconsin
REV A	JLL	13/04/01		