CMOS Analog Switches

The HI-300 thru HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Intersil dielectric isolation process. These switches feature break before-make switching, (HI-301, HI-303 and HI-307 only), low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few mW for the HI-300 thru HI-303, a few hundred mW for the HI-307).

The HI-300 thru HI-303 are TTL compatible and have a logic “0” condition with an input less than 0.8V and a logic “1” condition with an input greater than 4V. The HI-307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic “1” input.)

Features

- Analog Signal Range (±15V Supplies) ............... ±15V
- Low Leakage at 25°C ............................. 40pA
- Low Leakage at 125°C .......................... 1nA
- Low On Resistance at 25°C ..................... 35Ω
- Break-Before-Make Delay ...................... 60ns
- Charge Injection .............................. 30pC
- TTL, CMOS Compatible
- Symmetrical Switch Elements
- Low Operating Power (Typ for HI-300 thru HI-303) . . . 1.0mW

Applications

- Sample and Hold (i.e., Low Leakage Switching)
- Op Amp Gain Switching (i.e., Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Functional Diagram

Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TEMP. RANGE (°C)</th>
<th>PACKAGE</th>
<th>PKG. NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>HI1-0300-2</td>
<td>-55 to 125</td>
<td>14 Ld CERDIP</td>
<td>F14.3</td>
</tr>
<tr>
<td>HI9P0301-5</td>
<td>0 to 75</td>
<td>14 Ld SOIC</td>
<td>M14.15</td>
</tr>
<tr>
<td>HI1-0303-2</td>
<td>-55 to 125</td>
<td>14 Ld CERDIP</td>
<td>F14.3</td>
</tr>
<tr>
<td>HI1-0303-5</td>
<td>0 to 75</td>
<td>14 Ld CERDIP</td>
<td>F14.3</td>
</tr>
<tr>
<td>HI3-0303-5</td>
<td>0 to 75</td>
<td>14 Ld PDIP</td>
<td>E14.3</td>
</tr>
<tr>
<td>HI9P0303-5</td>
<td>0 to 75</td>
<td>14 Ld SOIC</td>
<td>M14.15</td>
</tr>
<tr>
<td>HI9P0303-9</td>
<td>-40 to 85</td>
<td>14 Ld SOIC</td>
<td>M14.15</td>
</tr>
<tr>
<td>HI1-0307-5</td>
<td>0 to 75</td>
<td>14 Ld CERDIP</td>
<td>F14.3</td>
</tr>
</tbody>
</table>

Pinouts

Switch States Shown For A Logic “1” Input

DUAL SPST HI-300 (CERDIP)  
( TOP VIEW )

SPST HI-301 (SOIC)  
( TOP VIEW )

DUAL SPDT HI-303 (PDIP, CERDIP, SOIC)  
( TOP VIEW )

<table>
<thead>
<tr>
<th>LOGIC</th>
<th>SW1</th>
<th>SW2</th>
<th>SW3</th>
<th>SW4</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>ON</td>
<td>OFF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site http://www.intersil.com
Absolute Maximum Ratings

Voltage Between Supplies (V+ to V-) ........................................... 44V (±22V)
Digital Input Voltage .......................................................... (V+) +4V to (V-) -4V
Analog Input Voltage .......................................................... (V+) +1.5V to (V-) -1.5V
Typical Derating Factor ...................................................... 1.5mA/MHz Increase in ICCOP
ESD Classification ............................................................ Class 1

Thermal Information

<table>
<thead>
<tr>
<th>Package</th>
<th>θJA (°C/W)</th>
<th>θJC (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CERDIP</td>
<td>95</td>
<td>40</td>
</tr>
<tr>
<td>PDIP</td>
<td>100</td>
<td>N/A</td>
</tr>
<tr>
<td>SOIC</td>
<td>120</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Operating Conditions

Temperature Range

- HI-3XX-2: -55°C to 125°C
- HI-3XX-5: 0°C to 75°C
- HI-3XX-9: -40°C to 85°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θJA is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEMP (°C)</th>
<th>-2</th>
<th>-5, -9</th>
</tr>
</thead>
<tbody>
<tr>
<td>PARAMETER</td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
</tbody>
</table>

DYNAMIC CHARACTERISTICS

- Switch ON Time, tON (Note 13)
- Switch OFF Time, tOFF (Note 13)
- Break-Before-Make Delay, tOPEN (Note 15)
- Charge Injection Voltage, ΔV (Note 7)
- OFF Isolation (Note 6)
- Digital Input Capacitance, CIN

DIGITAL INPUT CHARACTERISTICS

- Input Low Level, VINL (Note 13)
- Input High Level, VINH (Note 13)
- Input Low Level, VNIL (Note 14)
- Input High Level, VINHL (Note 14)
- Input Leakage Current (Low), IINL (Note 5)
- Input Leakage Current (High), IINH (Note 5)

ANALOG SWITCH CHARACTERISTICS

- Analog Signal Range
- ON Resistance, rON (Note 2)
- OFF Input Leakage Current, IS(Off) (Note 3)
- OFF Output Leakage Current, ID(Off) (Note 3)
- ON Leakage Current, ID(On) (Note 4)

POWER SUPPLY CHARACTERISTICS

- Current, I+ (Notes 8, 13)

CAUTION: Supplies = +15V, -15V, VIN = Logic Input. HI-300 thru HI-303: VIN for Logic “1” = 4V, for Logic “0” = 0.8V. HI-307: VIN for Logic “1” = 11V, for Logic “0” = 3.5V, Unless Otherwise Specified
Electrical Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEMP (°C)</th>
<th>-2</th>
<th>-5, -9</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current, I- (Notes 8, 13)</td>
<td>25</td>
<td>-</td>
<td>0.01</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Full</td>
<td>-</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Current, I- (Notes 9, 13)</td>
<td>25</td>
<td>-</td>
<td>0.01</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Full</td>
<td>-</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Current, I- (Notes 9, 13)</td>
<td>25</td>
<td>-</td>
<td>0.01</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Full</td>
<td>-</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Current, I- (Notes 10, 14)</td>
<td>25</td>
<td>-</td>
<td>0.01</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Full</td>
<td>-</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Current, I- (Notes 10, 14)</td>
<td>25</td>
<td>-</td>
<td>0.01</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Full</td>
<td>-</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Current, I- (Notes 11, 14)</td>
<td>25</td>
<td>-</td>
<td>0.01</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Full</td>
<td>-</td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Current, I- (Notes 11, 14)</td>
<td>25</td>
<td>-</td>
<td>0.01</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Full</td>
<td>-</td>
<td>-</td>
<td>100</td>
</tr>
</tbody>
</table>

NOTES:
2. $V_S = \pm 10V, I_{OUT} = \pm 10mA$. On resistance derived from the voltage measured across the switch under these conditions.
3. $V_S = \pm 14V, V_D = \pm 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}, f = 500kHz, C_L = 15pF, R_L = 1K$.
7. $V_S = 0V, C_L = 10nF$, Logic Drive = 5V pulse (HI-300 - 303), 15V pulse (HI-307). Switches are symmetrical; S and D may be interchanged. Charge Injection = $Q = C_L \times \Delta V$.
8. $V_{IN} = 4V$ (one input, all other inputs = 0V).
9. $V_{IN} = 0.8V$ (all inputs).
10. $V_{IN} = 15V$ (all inputs).
11. $V_{IN} = 0V$ (all inputs).
12. To drive from DTL/TTL circuits, pullup resistors to +5V supply are recommended.
13. HI-300 thru HI-303 only.
14. HI-307 only.
15. HI-301, HI-303, HI-307 only.

Test Circuits and Waveforms

<table>
<thead>
<tr>
<th>SWITCH TYPE</th>
<th>$V_{INH}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>HI-300 thru HI-303</td>
<td>4V</td>
</tr>
<tr>
<td>HI-307</td>
<td>15V</td>
</tr>
</tbody>
</table>
Test Circuits and Waveforms (Continued)

**FIGURE 2A. TEST CIRCUIT**

**FIGURE 2B. TTL LOGIC INPUT**

**FIGURE 2C. CMOS LOGIC INPUT**

**FIGURE 2D. \( V_{\text{ANALOG}} = 10V \)**

**FIGURE 2E. \( V_{\text{ANALOG}} = 5V \)**

**FIGURE 2F. \( V_{\text{ANALOG}} = 0V \)**

**FIGURE 2G. \( V_{\text{ANALOG}} = -5V \)**

**FIGURE 2H. \( V_{\text{ANALOG}} = -10V \)**

**NOTE:**

16. If \( R_{\text{GEN}}, R_L \) or \( C_L \) is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 2. SWITCHING WAVEFORMS FOR VARIOUS ANALOG INPUT VOLTAGES
Test Circuits and Waveforms (Continued)

<table>
<thead>
<tr>
<th>SWITCH TYPE</th>
<th>V_{INH}</th>
</tr>
</thead>
<tbody>
<tr>
<td>HI-301, HI-303</td>
<td>5V</td>
</tr>
<tr>
<td>HI-307</td>
<td>15V</td>
</tr>
</tbody>
</table>

Typical Performance Curves

**FIGURE 4.** $r_{DS(on)}$ vs $V_D$

- $V_+ = +15V, V_- = -15V$
- $T_A = 25^\circ C$
- $A: V_+ = +15V, V_- = -15V$
- $B: V_+ = +10V, V_- = -10V$
- $C: V_+ = +7.5V, V_- = -7.5V$
- $D: V_+ = +5V, V_- = -5V$

**FIGURE 5.** $r_{DS(on)}$ vs $V_D$

- $V_+ = +15V, V_- = -15V$
- $T_A = 25^\circ C$
- $V_+ = +10V, V_- = -10V$
- $V_+ = +7.5V, V_- = -7.5V$
- $V_+ = +5V, V_- = -5V$
- $V_+ = +15V, V_- = -15V$
- $V_+ = +10V, V_- = -10V$
- $V_+ = +7.5V, V_- = -7.5V$
- $V_+ = +5V, V_- = -5V$

**FIGURE 6.** Device Power Dissipation vs Switching Frequency (Single Logic Input)

- $V_+ = +15V, V_- = -15V$
- $T_A = 25^\circ C, V_S = 15V, R_L = 2K$
- $V_+ = +15V, V_- = -15V$
- $C_{LOAD} = 30pF, V_S = 1V RMS$
- $R_L = 100\Omega$
- $R_L = 1k\Omega$

**FIGURE 7.** Off Isolation vs Frequency

- $V_+ = +15V, V_- = -15V$
- $V_+ = +10V, V_- = -10V$
- $V_+ = +7.5V, V_- = -7.5V$
- $V_+ = +5V, V_- = -5V$
Typical Performance Curves  (Continued)

**FIGURE 8. I_{S(ON)} OR I_{D(ON)} vs TEMPERATURE†**

† The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

**FIGURE 9. I_{D(ON)} vs TEMPERATURE†**

**FIGURE 10. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE**

**FIGURE 11. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE**

**FIGURE 12. SWITCHING TIME vs TEMPERATURE, HI-300 THRU HI-303**

**FIGURE 13. SWITCHING TIME vs TEMPERATURE, HI-307**
Typical Performance Curves (Continued)

FIGURE 14. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE, HI-300 THRU HI-303

FIGURE 15. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE, HI-307

FIGURE 16. SWITCHING TIME AND BREAK-BEFORE-MAKE TIME vs POSITIVE SUPPLY VOLTAGE, HI-300 THRU HI-303

FIGURE 17. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE, HI-307

FIGURE 18. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE